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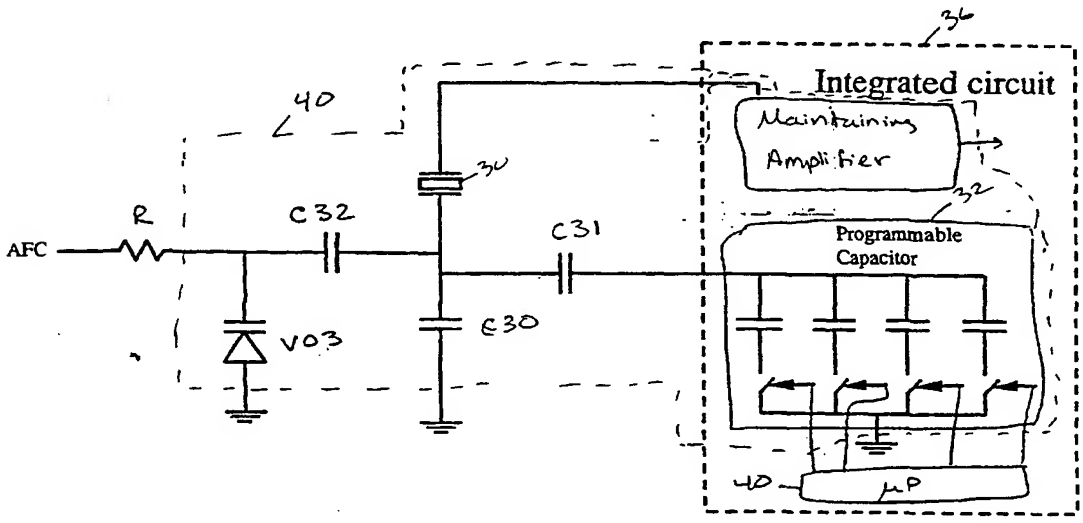
(54) Title: APPARATUS AND METHOD FOR CHANGING CRYSTAL OSCILLATOR FREQUENCY



(57) Abstract: A programmable capacitor array is used to trim the frequency of a crystal oscillator for initial offset. An apparatus includes the crystal oscillator and an integrated circuit (36) is coupled to the crystal (30) of the oscillator. The programmable capacitor array (32) is formed on the integrated circuit and is coupled to the crystal (30) and is responsive to a signal for setting the capacitance of the capacitor array to one of a number of capacitance values. A discrete controllable capacitance device (V03) not one the integrated circuit is coupled to the crystal (30) and is responsive to a control signal (AFC) to change its capacitance. The crystal oscillator frequency is dependent on the capacitances of both the programmable capacitor array (32) and the discrete capacitor (V03).

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APPARATUS AND METHOD FOR CHANGING CRYSTAL OSCILLATOR FREQUENCY

Cross Reference to Related Application

This application claims priority from Provisional Application No. 60/161,582, filed October 26, 1999, the contents of which are expressly incorporated herein by reference for all purposes.

Background of the Invention

This invention relates to the use of a crystal oscillator and the adjustment of the frequency of the oscillator.

It is generally known in systems that include a crystal oscillator that the frequency of the oscillator can be changed by including in the oscillator a varactor coupled to a crystal, and then applying a voltage to the varactor. A varactor is a diode with a capacitance that changes in response to an applied voltage, and thus can be considered a voltage-controlled variable capacitor. In systems that use a varactor for this purpose, a digital to analog converter (DAC) is typically provided as part of a closed loop system to provide a voltage to the varactor to change the capacitance. As a result of this applied voltage, the center frequency of the oscillator is changed to a desired value. This adjustment can be made on an ongoing basis.

U.S. Patent Nos. 5,117,206 and 5,204,975 shows methods for digitally correcting frequency on an ongoing basis to compensate for changes in temperature. As indicated in the latter patent, the crystal oscillator is coupled to a capacitor trimming bank, which is coupled to a capacitor switching bank. The switches in the switching bank are controlled in response to temperature sensing by a temperature sensor. The temperature sensor is coupled to an analog to digital converter (ADC), which is coupled to a PROM, which, in turn, is coupled to

a latch. The control of the frequency of the crystal oscillator is thus continuously updated to adjust for changes in temperature. In this case, the capacitor bank is on the input side and thus appears to be discrete components. In the former patent, temperature compensation is performed on the output side of the crystal for controlling capacitance on an ongoing basis to compensate for temperature. In each case, the group of capacitors essentially replaces the functionality of a varactor used in the manner described above.

Summary of the Invention

The present invention includes a system and method for the initial trimming of the frequency of a crystal oscillator by providing in the oscillator circuitry an integrated programmable capacitor array on a chip that uses the oscillating signal. The array preferably has a number of capacitors in parallel, with each capacitor in the array formed in series with an integrated switch. Consequently one or more of the capacitors can be turned on or off to produce a desired capacitance and, thus, a desired frequency adjustment. This adjustment is preferably made one time for initial offset adjustment, after which time, a control signal to the capacitor array may be kept constant, and not for ongoing compensation. A varactor may provide further adjustment or compensation on an ongoing basis if needed. The signal to the switches may be provided from a microprocessor for providing the trimming function. The capacitor array is preferably integrated in silicon, with the chip being part of a synthesizer circuit. The capacitors may, for example, be n-well devices or doped polysilicon layers separated by an oxide layer, and the switches may be grounded drain NMOS switches.

The system and method of the present invention can potentially replace a varactor with an array of capacitors that can be individually controlled, and therefore no varactor or DAC may be needed. Alternatively and preferably, a varactor and DAC are used for ongoing adjustment, and the requirements of the varactor or DAC may be relaxed; in other words,

because of the initial trimming provided from the array, the design and tolerances of the varactor may not need to be as precise as they may be otherwise. Thus, in another aspect, the invention includes an oscillator with a programmable capacitor on a chip and responsive to a digital signal for use only for initial adjustment offset, and also a discrete component varactor responsive to an analog signal that may be used for compensation or trimming on an ongoing basis. With a programmable array with capacitors having 10% tolerance, it has been found that the frequency can be adjusted within a generally acceptable 10 parts per million (ppm), with average resolution steps of 3.1 ppm. Other features and advantages will become apparent from the following detailed description, drawings, and claims.

Brief Description of the Drawings

Figs. 1-6 are schematics of embodiments of the present invention.

Detailed Description

Referring to Fig. 1, a circuit 10 has a crystal 12 coupled to capacitor C10 between the crystal and ground. Capacitor C10 is in parallel with a series combination of capacitor C11 and a programmable capacitor 14. Capacitors C10 and C11 as shown here have fixed capacitances. Crystal 12 is also coupled to a generally known maintaining amplifier 16 on an integrated circuit chip 18. Maintaining amplifier 16 essentially maintains oscillations by replacing energy lost through resistive components. Programmable capacitor 14 is preferably also integrated and formed on chip 18, e.g., with n-well structures or parallel doped polysilicon plates with oxide as the dielectric and in series with integrated switches. Crystal 12, capacitors C10, C11, and 14, and maintaining amplifier 16 thus form a crystal oscillator 24 that provides an oscillating signal that is a function of the capacitances and the structure of the crystal.

By controlling the capacitance on programmable capacitor 14, oscillator 24 can be trimmed. According to a method of the present invention, and in one particular embodiment for use with a synthesizer in a GSM device, oscillator 24 preferably provides a signal at 13 MHz. After the circuit is made, the frequency of oscillator 24 is measured, and then programmable capacitor 14 is adjusted to trim the output of oscillator 24 to a precise value of 13 MHz. Programmable capacitor 14 is preferably controlled by a digital signal 22 from a microprocessor 20 and is essentially a one-time initial offset trimming function. In other words, once the trimming has been performed, signal 22 to programmable capacitor 14 need not be changed. Signal 22 thus could be, for example, a 4-bit signal, with each bit controlling one switch. Other frequencies could, alternatively, be used.

Fig. 2 is another embodiment with substantial similarities to Fig. 1, except that a crystal 26 is in parallel to capacitor C20 and also in parallel to a series connection of capacitors C21 and programmable capacitor 14 to form oscillator 28.

Referring to Fig. 3, a crystal 30 is coupled through ground to capacitor C30 which is in parallel with a series of capacitor C31 and programmable capacitor 32. Oscillator 30 is also coupled through capacitor C32 to a varactor V03 coupled to ground. Voltage to varactor V03 is provided by an automatic frequency control (AFC) signal through a resistor R. The AFC signal would be provided from a DAC as part of a closed loop for controlling the frequency of the oscillator.

Programmable capacitor 32 is formed on integrated circuit 36 and, in this particular embodiment, has four capacitors in parallel, with each of the four capacitors in series with a switch. These capacitors are integrated, e.g., as n-well capacitors or formed from polysilicon layers separated by oxide, with grounded drain NMOS switches in series. The capacitors can all have the same value, for example, 5.5 pF each. Thus, in this embodiment, an integrated programmable capacitor 14 and a discrete varactor V03 are both used, with programmable

capacitor 14 under digital control for initial offset and varactor V03 responsive to an analog signal for ongoing adjustment. The signal that is provided to the four switches is thus a 4-bit signal that is preferably provided from a microprocessor 40 as one of a number of functions served by the microporocesser.

It has been found that using a four capacitor array with external (off-chip) and internal (programmable) capacitors having a tolerance of ten (10%) percent, the frequency of the crystal can be set with a tolerance of +/- 10 ppm to compensate for the crystal adjustment offset (i.e., initial tolerance). A typical step size of 3.1 ppm was achieved, with a worst case of 4.4 ppm.

Figs. 4-6 show additional embodiments of crystal oscillators 50, 52, and 54 according to the present invention for providing an initial trim. These schematics show a combination of on-chip and off-chip components. The programmable capacitor could potentially be any one of capacitors C40, C41, C50, C51, C60, or C61 in these embodiments, although some selections may be less desirable (e.g., if they would require an additional pin on a chip). In each case, the other capacitance would be fixed. In each case, the programmable capacitor is integrated on the chip. Note that Figs. 5 and 6 show the use of a varactor with a voltage signal, V, for controlling the capacitance on the varactor, thus indicating that there would be closed loop control of the capacitance after the initial trim. The varactor and any fixed capacitors would be off-chip. Figs. 4 and 6 are different from Fig. 5 in that the crystal is grounded on one side.

Having described the preferred embodiments of the present invention, it should be apparent that modifications can be made without departing from the scope of the invention as defined by the appended claims. For example, other specific frequencies could be used; generally a crystal can be cut to produce a desired frequency. Other integration techniques and methods could be used for making integrated capacitors and switches.

What is claimed is:

Claims

1. An apparatus including a crystal oscillator with a crystal and a capacitor that can be adjusted to control a frequency of an oscillating signal from the crystal oscillator, and an integrated circuit coupled to the crystal for receiving the oscillating signal, characterized in that:

an integrated programmable capacitor is formed on the integrated circuit and is coupled to the crystal and is responsive to a signal for causing the capacitance of the programmable capacitor to be set to one of a number of capacitance values;

a discrete controllable capacitance device not on the integrated circuit is coupled to the crystal and is responsive to a control signal for causing the capacitance of the device to be controlled;

wherein the oscillating signal provided to the integrated circuit has a frequency that depends in part on the capacitances of both the controllable discrete capacitor device and the integrated programmable capacitor.

2. The apparatus of claim 1, wherein the programmable capacitor includes a plurality of integrated capacitors in parallel and a plurality of integrated switches, with one switch in series with each of a number of the integrated capacitors.

3. The apparatus of claim 2, wherein the integrated capacitors are each n-well devices.

4. The apparatus of claim 2, wherein the integrated capacitors each have two layers of polysilicon separated by an oxide layer.

5. The apparatus of claim 2, wherein there are four integrated capacitors and four switches, and wherein the programmable capacitor is controlled by a 4-bit digital signal.

6. The apparatus of any of the previous claims, wherein the controllable capacitance device includes a varactor responsive to an analog voltage signal for changing its capacitance.

7. The apparatus of any of the previous claims, wherein the integrated circuit includes a maintaining amplifier for providing energy to maintain the oscillating signal.

8. The apparatus of any of the previous claims, wherein the integrated circuit is a synthesizer for a GSM device.

9. The apparatus of any of the previous claims, wherein the programmable capacitor is used for initial offset tuning of the frequency of the oscillating signal, and the controllable capacitance device is used for ongoing adjustment of the frequency.

10. The apparatus of any of the previous claims, further comprising at least one fixed capacitor coupled to the crystal, wherein the frequency of the oscillating signal is also a function of the capacitance of the one or more fixed capacitors.

11. A method for use with a crystal oscillator having a crystal coupled to a variable capacitance and coupled to an integrated circuit including detecting a frequency of

oscillation of the crystal oscillator and adjusting a capacitance to alter the frequency of the crystal oscillator to a desired frequency, characterized in that:

a programmable capacitor is formed on an integrated circuit and is coupled to the crystal;

a discrete controllable capacitor not on the integrated circuit;

the programmable capacitor is controlled for initial crystal adjustment offset; and

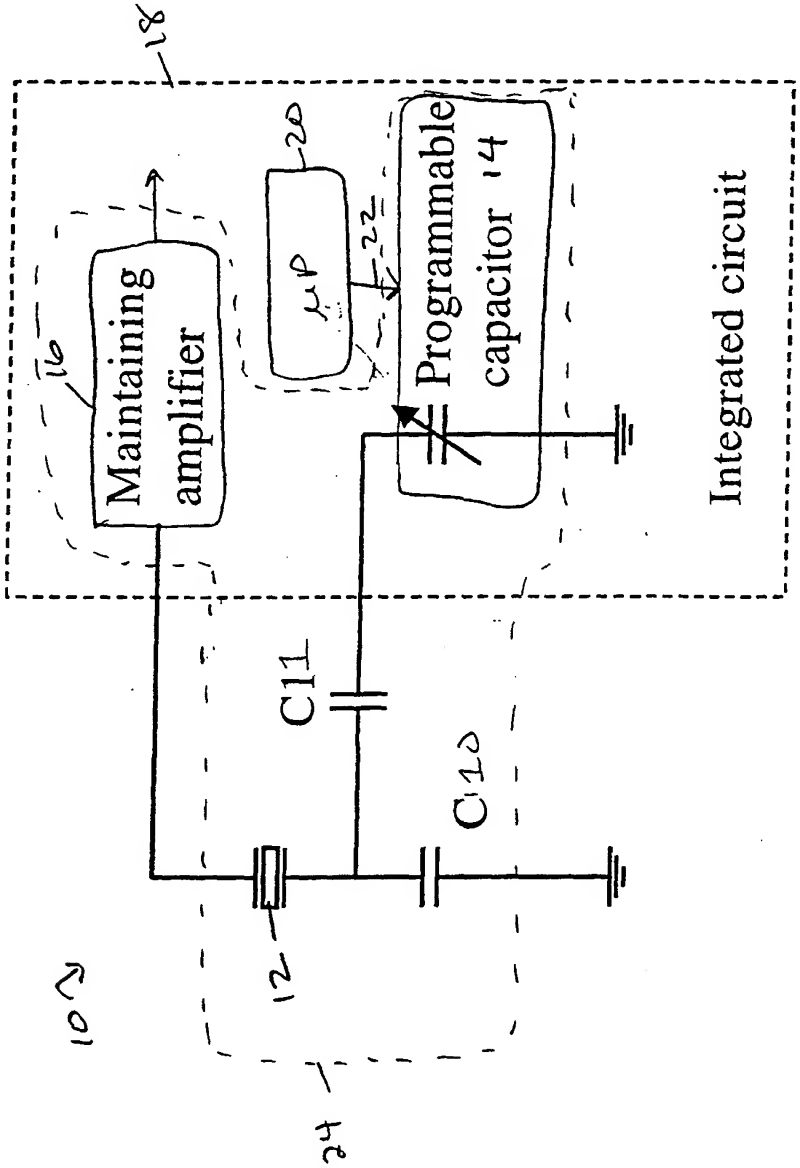
thereafter, on an ongoing basis, the discrete controllable capacitor is controlled to compensate for changes in the frequency of oscillation from the crystal oscillator during operation so that the frequency maintains the desired frequency.

12. The method of claim 11, further comprising forming a plurality of integrated capacitors in parallel, and forming switches, with one in series with each integrated capacitor, and the controlling includes providing digital control signals to the switches to control the capacitance of the programmable capacitor.

13. The method of claim 12, wherein controlling the programmable capacitor includes providing a digital signal to one or more switches that are integrated as part of the programmable capacitor.

14. The method of any of the previous claims, wherein the controlling steps are performed so that the desired frequency is 13 MHz, the integrated circuit including a GSM synthesizer.

15. The method of any of the previous claims, wherein controlling the controllable capacitor includes providing an analog signal from a digital to analog converter.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Maintaining amplifier
16
μP
20
22
Programmable capacitor 14
Integrated circuit
C11
C12
12
10
24

FIG. 1

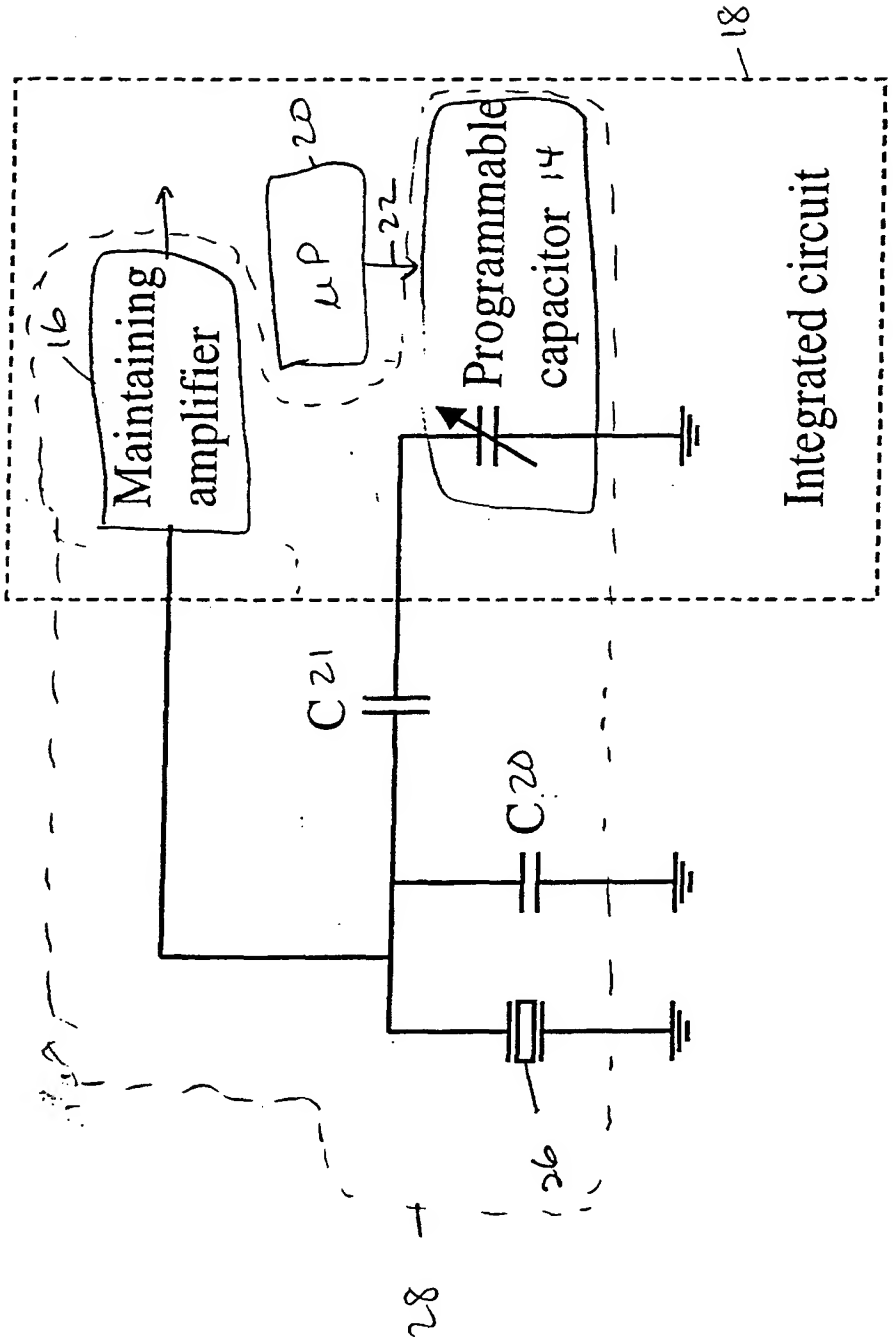
18
Integrated circuit
Maintaining amplifier
16
μP
20
22
Programmable capacitor 14
C21
C20
26
28

FIG. 2

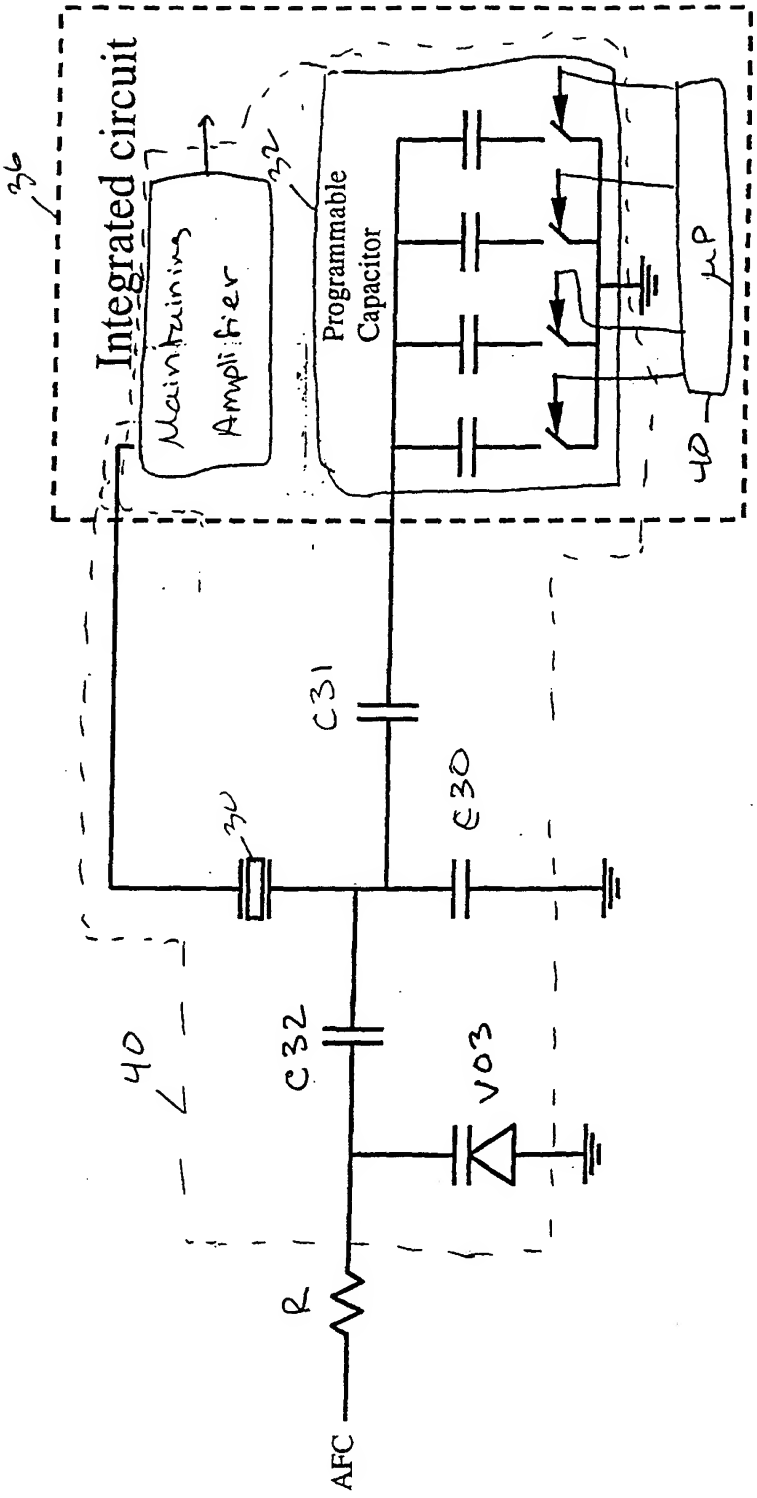
Integrated circuit
Maintaining Amplifier
Programmable Capacitor
μP
36
32
40
C31
C30
C32
V03
R
AFC

FIG. 3

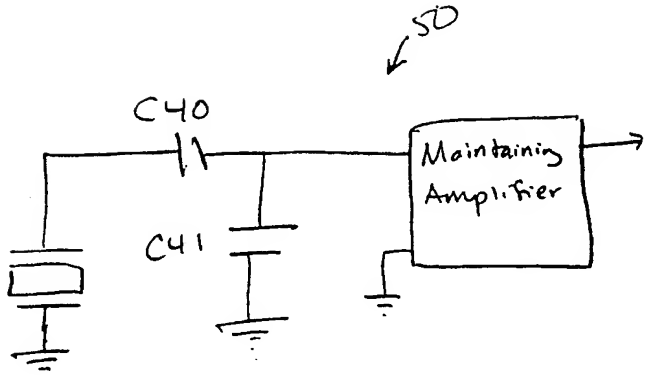

FIG. 4

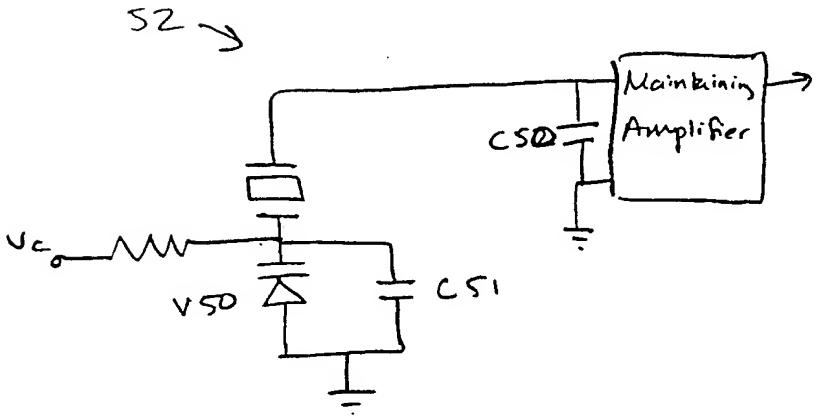

FIG. 5

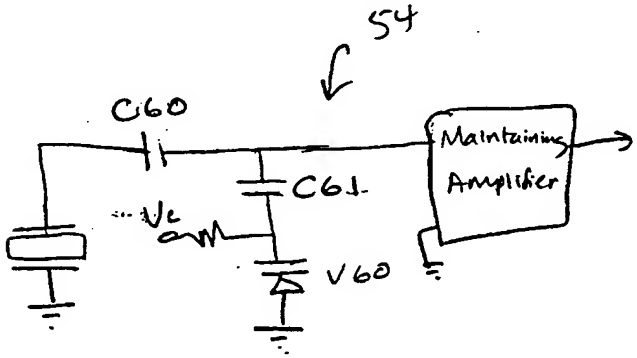

FIG. 6

INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/US 00/29437

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03B5/32 H03J7/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03B H03L H03J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
INSPEC, COMPENDEX, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 745 012 A (SHIMODAIRA KAZUHIKO ET AL) 28 April 1998 (1998-04-28) column 1, line 11 - line 22 column 1, line 67 -column 2, line 4 column 7, line 8 -column 8, line 43 column 9, line 1 - line 12 column 9, line 43 -column 11, line 65 figures 1-3,5,8-13	1-15

X	US 5 936 474 A (ROUSSELIN SAMUEL) 10 August 1999 (1999-08-10) the whole document	1-15

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 January 2001	07/02/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Balbinot, H

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Int. ional Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 204 975 A (SHIGEMORI MIKIO) 20 April 1993 (1993-04-20) cited in the application column 1, line 9 - line 16 column 4, line 66 -column 7, line 58; figures 3-5,7-10	1-5,7,8, 10-14
A	US 5 117 206 A (IMAMURA YOICHI) 26 May 1992 (1992-05-26) cited in the application column 1, line 7 - line 14 column 3, line 61 -column 10, line 44; figures	1-5,7,8, 10-14

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ional Application No
PCT/US 00/29437

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		EP 0431887 A	12-06-1991

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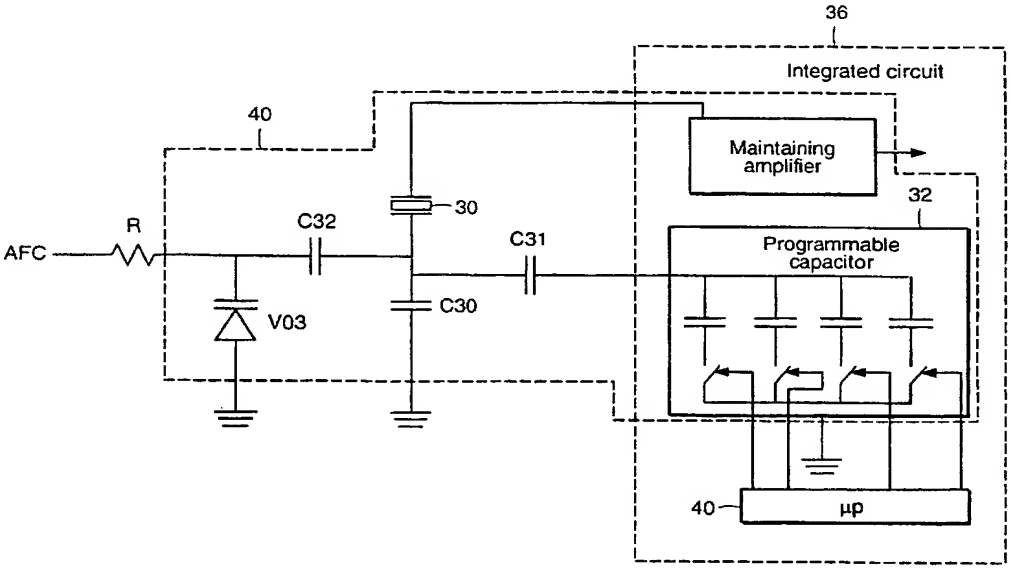

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U.S. Patent Nos. 5,117,206 and 5,204,975 shows methods for digitally correcting frequency on an ongoing basis to compensate for changes in temperature. As indicated in the latter patent, the crystal oscillator is coupled to a capacitor trimming bank, which is coupled to a capacitor switching bank. The switches in the switching bank are controlled in response to temperature sensing by a temperature sensor. The temperature sensor is coupled to an analog to digital converter (ADC), which is coupled to a PROM, which, in turn, is coupled to

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Summary of the Invention

The present invention includes a system and method for the initial trimming of the frequency of a crystal oscillator by providing in the oscillator circuitry an integrated programmable capacitor array on a chip that uses the oscillating signal. The array preferably has a number of capacitors in parallel, with each capacitor in the array formed in series with an integrated switch. Consequently one or more of the capacitors can be turned on or off to produce a desired capacitance and, thus, a desired frequency adjustment. This adjustment is preferably made one time for initial offset adjustment, after which time, a control signal to the capacitor array may be kept constant, and not for ongoing compensation. A varactor may provide further adjustment or compensation on an ongoing basis if needed. The signal to the switches may be provided from a microprocessor for providing the trimming function. The capacitor array is preferably integrated in silicon, with the chip being part of a synthesizer circuit. The capacitors may, for example, be n-well devices or doped polysilicon layers separated by an oxide layer, and the switches may be grounded drain NMOS switches.

The system and method of the present invention can potentially replace a varactor with an array of capacitors that can be individually controlled, and therefore no varactor or DAC may be needed. Alternatively and preferably, a varactor and DAC are used for ongoing adjustment, and the requirements of the varactor or DAC may be relaxed; in other words,

because of the initial trimming provided from the array, the design and tolerances of the varactor may not need to be as precise as they may be otherwise. Thus, in another aspect, the invention includes an oscillator with a programmable capacitor on a chip and responsive to a digital signal for use only for initial adjustment offset, and also a discrete component varactor responsive to an analog signal that may be used for compensation or trimming on an ongoing basis. With a programmable array with capacitors having 10% tolerance, it has been found that the frequency can be adjusted within a generally acceptable 10 parts per million (ppm), with average resolution steps of 3.1 ppm. Other features and advantages will become apparent from the following detailed description, drawings, and claims.

Brief Description of the Drawings

Figs. 1-6 are schematics of embodiments of the present invention.

Detailed Description

Referring to Fig. 1, a circuit 10 has a crystal 12 coupled to capacitor C10 between the crystal and ground. Capacitor C10 is in parallel with a series combination of capacitor C11 and a programmable capacitor 14. Capacitors C10 and C11 as shown here have fixed capacitances. Crystal 12 is also coupled to a generally known maintaining amplifier 16 on an integrated circuit chip 18. Maintaining amplifier 16 essentially maintains oscillations by replacing energy lost through resistive components. Programmable capacitor 14 is preferably also integrated and formed on chip 18, e.g., with n-well structures or parallel doped polysilicon plates with oxide as the dielectric and in series with integrated switches. Crystal 12, capacitors C10, C11, and 14, and maintaining amplifier 16 thus form a crystal oscillator 24 that provides an oscillating signal that is a function of the capacitances and the structure of the crystal.

By controlling the capacitance on programmable capacitor 14, oscillator 24 can be trimmed. According to a method of the present invention, and in one particular embodiment for use with a synthesizer in a GSM device, oscillator 24 preferably provides a signal at 13 MHz. After the circuit is made, the frequency of oscillator 24 is measured, and then programmable capacitor 14 is adjusted to trim the output of oscillator 24 to a precise value of 13 MHz. Programmable capacitor 14 is preferably controlled by a digital signal 22 from a microprocessor 20 and is essentially a one-time initial offset trimming function. In other words, once the trimming has been performed, signal 22 to programmable capacitor 14 need not be changed. Signal 22 thus could be, for example, a 4-bit signal, with each bit controlling one switch. Other frequencies could, alternatively, be used.

Fig. 2 is another embodiment with substantial similarities to Fig. 1, except that a crystal 26 is in parallel to capacitor C20 and also in parallel to a series connection of capacitors C21 and programmable capacitor 14 to form oscillator 28.

Referring to Fig. 3, a crystal 30 is coupled through ground to capacitor C30 which is in parallel with a series of capacitor C31 and programmable capacitor 32. Oscillator 30 is also coupled through capacitor C32 to a varactor V03 coupled to ground. Voltage to varactor V03 is provided by an automatic frequency control (AFC) signal through a resistor R. The AFC signal would be provided from a DAC as part of a closed loop for controlling the frequency of the oscillator.

Programmable capacitor 32 is formed on integrated circuit 36 and, in this particular embodiment, has four capacitors in parallel, with each of the four capacitors in series with a switch. These capacitors are integrated, e.g., as n-well capacitors or formed from polysilicon layers separated by oxide, with grounded drain NMOS switches in series. The capacitors can all have the same value, for example, 5.5 pF each. Thus, in this embodiment, an integrated programmable capacitor 14 and a discrete varactor V03 are both used, with programmable

capacitor 14 under digital control for initial offset and varactor V03 responsive to an analog signal for ongoing adjustment. The signal that is provided to the four switches is thus a 4-bit signal that is preferably provided from a microprocessor 40 as one of a number of functions served by the microporocesser.

It has been found that using a four capacitor array with external (off-chip) and internal (programmable) capacitors having a tolerance of ten (10%) percent, the frequency of the crystal can be set with a tolerance of +/- 10 ppm to compensate for the crystal adjustment offset (i.e., initial tolerance). A typical step size of 3.1 ppm was achieved, with a worst case of 4.4 ppm.

Figs. 4-6 show additional embodiments of crystal oscillators 50, 52, and 54 according to the present invention for providing an initial trim. These schematics show a combination of on-chip and off-chip components. The programmable capacitor could potentially be any one of capacitors C40, C41, C50, C51, C60, or C61 in these embodiments, although some selections may be less desirable (e.g., if they would require an additional pin on a chip). In each case, the other capacitance would be fixed. In each case, the programmable capacitor is integrated on the chip. Note that Figs. 5 and 6 show the use of a varactor with a voltage signal, V, for controlling the capacitance on the varactor, thus indicating that there would be closed loop control of the capacitance after the initial trim. The varactor and any fixed capacitors would be off-chip. Figs. 4 and 6 are different from Fig. 5 in that the crystal is grounded on one side.

Having described the preferred embodiments of the present invention, it should be apparent that modifications can be made without departing from the scope of the invention as defined by the appended claims. For example, other specific frequencies could be used; generally a crystal can be cut to produce a desired frequency. Other integration techniques and methods could be used for making integrated capacitors and switches.

What is claimed is:

Claims

1. An apparatus including a crystal oscillator with a crystal and a capacitor that can be adjusted to control a frequency of an oscillating signal from the crystal oscillator, and an integrated circuit coupled to the crystal for receiving the oscillating signal, characterized in that:

an integrated programmable capacitor is formed on the integrated circuit and is coupled to the crystal and is responsive to a signal for causing the capacitance of the programmable capacitor to be set to one of a number of capacitance values;

a discrete controllable capacitance device not on the integrated circuit is coupled to the crystal and is responsive to a control signal for causing the capacitance of the device to be controlled;

wherein the oscillating signal provided to the integrated circuit has a frequency that depends in part on the capacitances of both the controllable discrete capacitor device and the integrated programmable capacitor.

2. The apparatus of claim 1, wherein the programmable capacitor includes a plurality of integrated capacitors in parallel and a plurality of integrated switches, with one switch in series with each of a number of the integrated capacitors.

3. The apparatus of claim 2, wherein the integrated capacitors are each n-well devices.

4. The apparatus of claim 2, wherein the integrated capacitors each have two layers of polysilicon separated by an oxide layer.

5. The apparatus of claim 2, wherein there are four integrated capacitors and four switches, and wherein the programmable capacitor is controlled by a 4-bit digital signal.

6. The apparatus of any of the previous claims, wherein the controllable capacitance device includes a varactor responsive to an analog voltage signal for changing its capacitance.

7. The apparatus of any of the previous claims, wherein the integrated circuit includes a maintaining amplifier for providing energy to maintain the oscillating signal.

8. The apparatus of any of the previous claims, wherein the integrated circuit is a synthesizer for a GSM device.

9. The apparatus of any of the previous claims, wherein the programmable capacitor is used for initial offset tuning of the frequency of the oscillating signal, and the controllable capacitance device is used for ongoing adjustment of the frequency.

10. The apparatus of any of the previous claims, further comprising at least one fixed capacitor coupled to the crystal, wherein the frequency of the oscillating signal is also a function of the capacitance of the one or more fixed capacitors.

11. A method for use with a crystal oscillator having a crystal coupled to a variable capacitance and coupled to an integrated circuit including detecting a frequency of

oscillation of the crystal oscillator and adjusting a capacitance to alter the frequency of the crystal oscillator to a desired frequency, characterized in that:

a programmable capacitor is formed on an integrated circuit and is coupled to the crystal;

a discrete controllable capacitor not on the integrated circuit;

the programmable capacitor is controlled for initial crystal adjustment offset; and

thereafter, on an ongoing basis, the discrete controllable capacitor is controlled to compensate for changes in the frequency of oscillation from the crystal oscillator during operation so that the frequency maintains the desired frequency.

12. The method of claim 11, further comprising forming a plurality of integrated capacitors in parallel, and forming switches, with one in series with each integrated capacitor, and the controlling includes providing digital control signals to the switches to control the capacitance of the programmable capacitor.

13. The method of claim 12, wherein controlling the programmable capacitor includes providing a digital signal to one or more switches that are integrated as part of the programmable capacitor.

14. The method of any of the previous claims, wherein the controlling steps are performed so that the desired frequency is 13 MHz, the integrated circuit including a GSM synthesizer.

15. The method of any of the previous claims, wherein controlling the controllable capacitor includes providing an analog signal from a digital to analog converter.

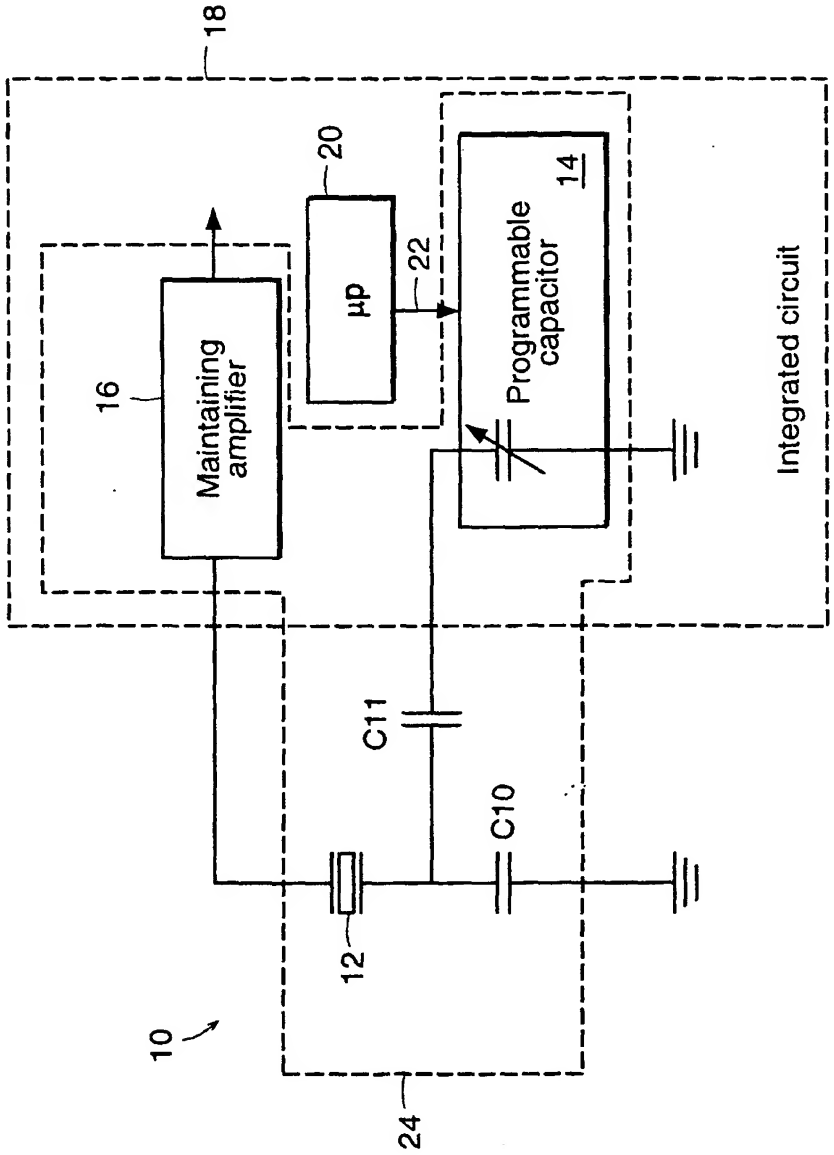
18
20
μp
22
Programmable capacitor
14
Integrated circuit
16
Maintaining amplifier
C11
C10
12
10
24

FIG. 1

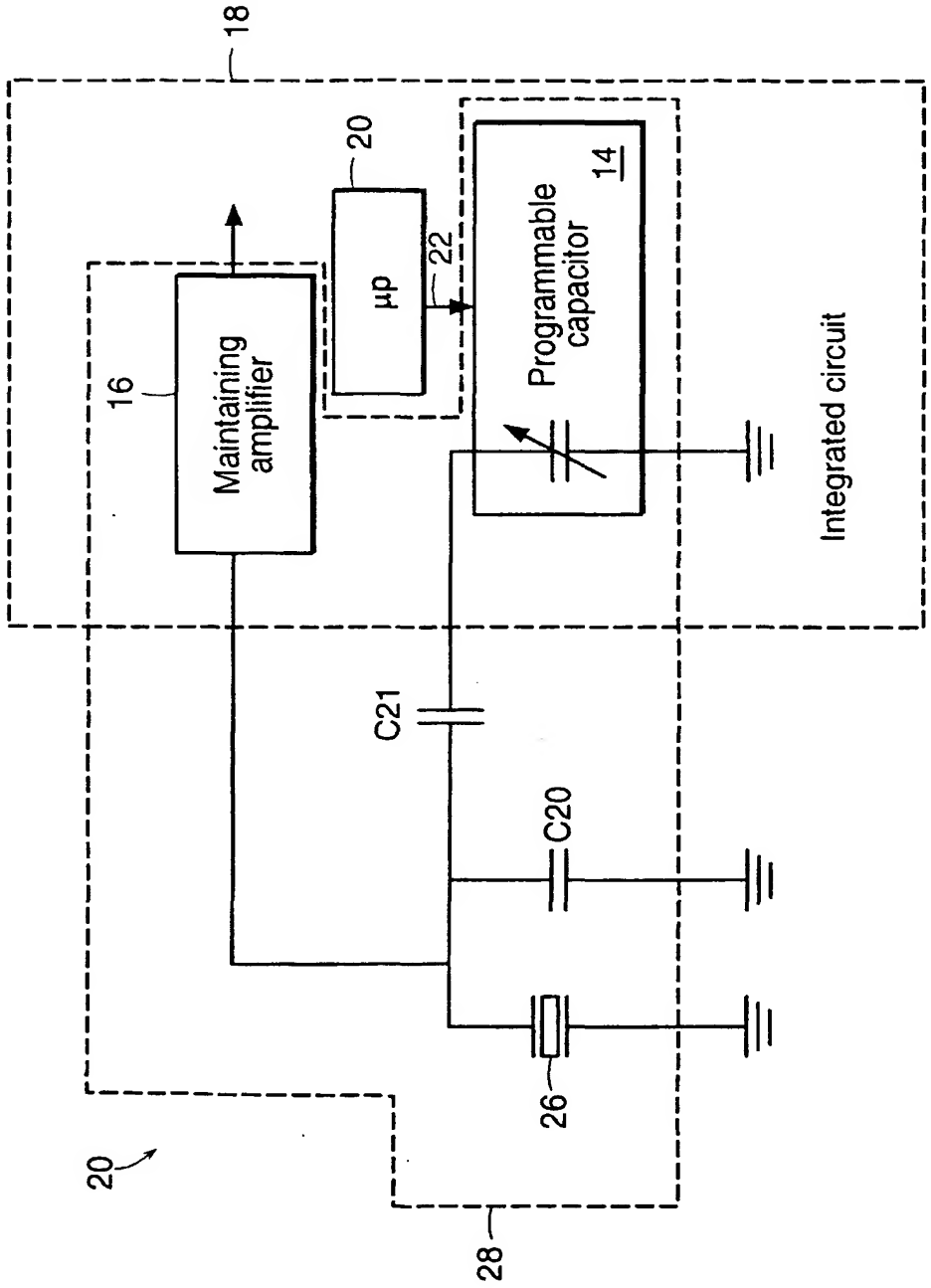
18
20
µp
22
Programmable capacitor
14
16
Maintaining amplifier
Integrated circuit
C21
C20
26
20
28

FIG. 2

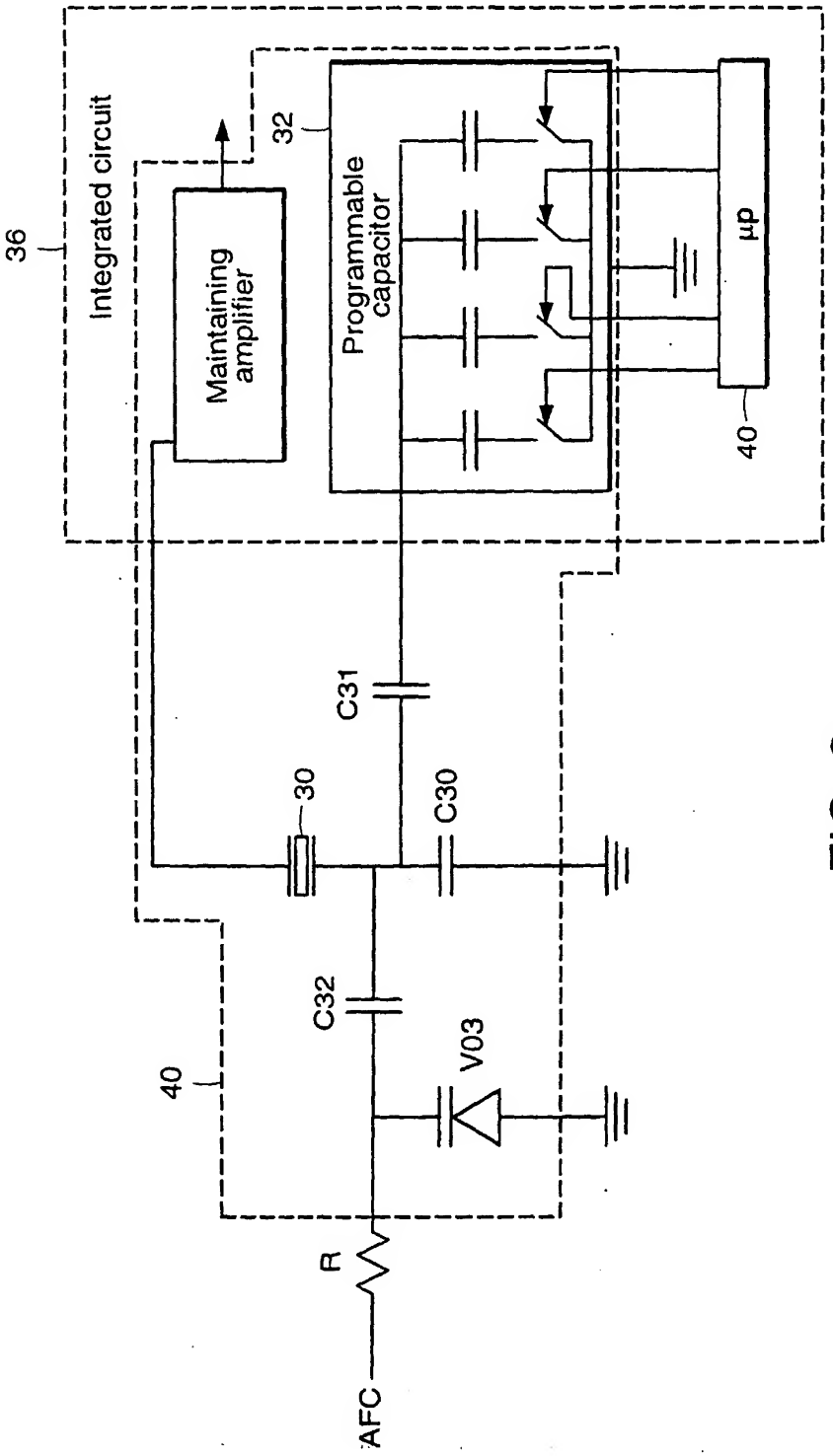
36
Integrated circuit
Maintaining amplifier
32
Programmable capacitor
µp
40
C31
30
C30
C32
V03
40
R
AFC

FIG. 3

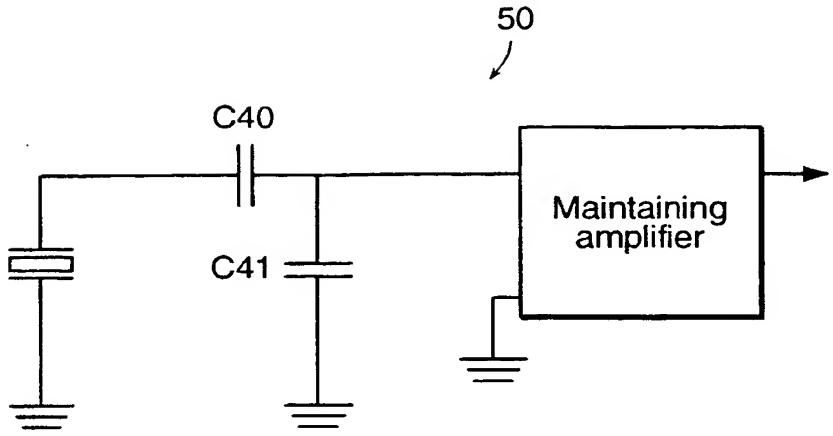

FIG. 4

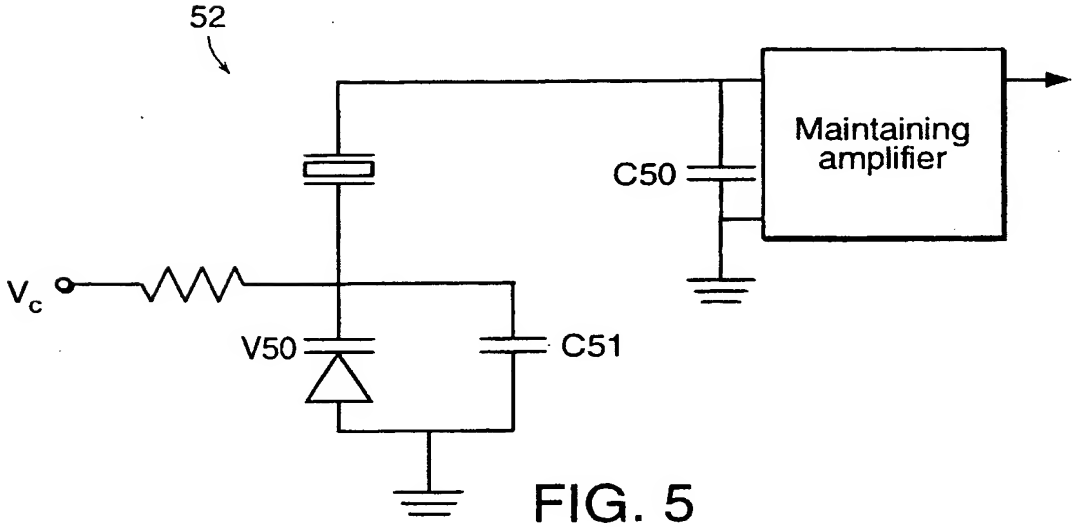

FIG. 5

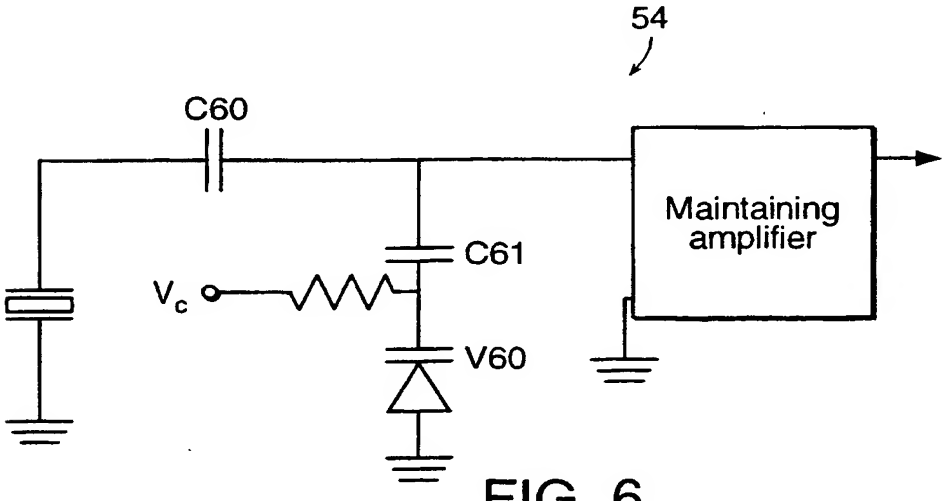

FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/29437

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03B5/32 H03J7/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03B H03L H03J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
INSPEC, COMPENDEX, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 745 012 A (SHIMODAIRA KAZUHIKO ET AL) 28 April 1998 (1998-04-28) column 1, line 11 - line 22 column 1, line 67 -column 2, line 4 column 7, line 8 -column 8, line 43 column 9, line 1 - line 12 column 9, line 43 -column 11, line 65 figures 1-3,5,8-13	1-15
X	US 5 936 474 A (ROUSSELIN SAMUEL) 10 August 1999 (1999-08-10) the whole document	1-15

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 January 2001	07/02/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Balbinot, H

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/29437

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 5 204 975 A (SHIGEMORI MIKIO) 20 April 1993 (1993-04-20) cited in the application column 1, line 9 - line 16 column 4, line 66 -column 7, line 58; figures 3-5,7-10	1-5,7,8, 10-14
A	US 5 117 206 A (IMAMURA YOICHI) 26 May 1992 (1992-05-26) cited in the application column 1, line 7 - line 14 column 3, line 61 -column 10, line 44; figures	1-5,7,8, 10-14

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